(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 February 2003 (27.02.2003)

PCT

(10) International Publication Number
WO 03/017336 A2

(51) International Patent Classification[7]: H01L 21/00

(21) International Application Number: PCT/US02/25680

(22) International Filing Date: 13 August 2002 (13.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/311,801 13 August 2001 (13.08.2001) US

(71) Applicant: AMBERWAVE SYSTEMS CORPORATION [US/US]; 13 Garabedian Drive, Salem, NH 03079 (US).

(72) Inventors: BULSARA, Mayank,; 62 Spring Street, Apt. 2L, Cambridge, MA 02141 (US). CURRIE, Matthew, T.; 8 Fletcher Road, Windham, NH 03087 (US). LOCHTEFELD, Anthony, J.; 29 Charnwood Road, Somerville, MA 02144 (US).

(74) Agent: US, Natasha; Testa, Hurwitz & Thibeault, LLP, High Street Tower, 125 High Street, Boston, MA 02110 (US).

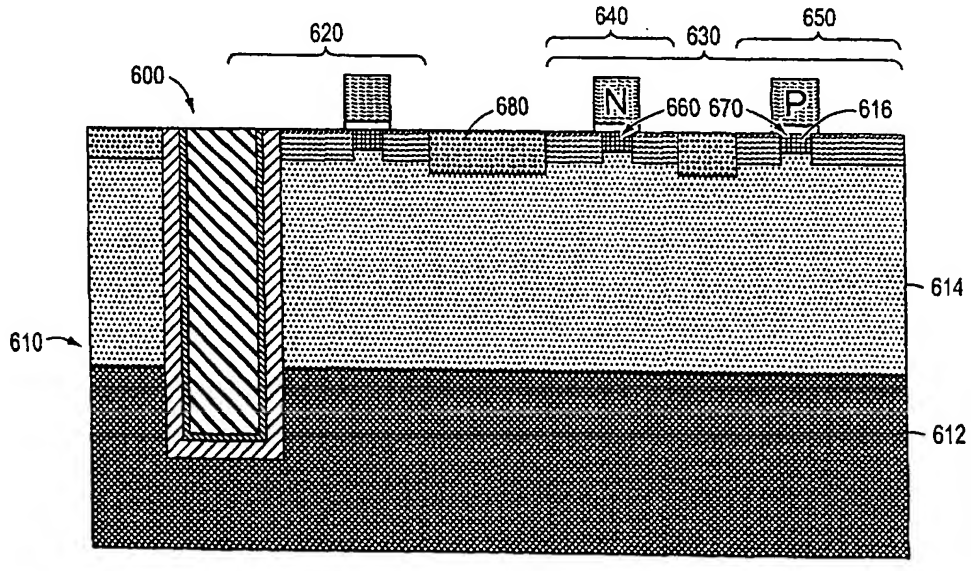
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: CONDENSATEURS A TRANCHEE POUR MEMOIRE DYNAMIQUE A ACCES ALEATOIRE



(57) Abstract: Cette invention concerne des condensateurs à tranchée pour mémoire dynamique à accès aléatoire formés, entre autres choses, par dépôt d'un matériau conducteur dans une tranchée ou par dopage de la région conductrice dans laquelle se situe la tranchée.

WO 03/017336 A2

DYNAMIC RANDOM ACCESS MEMORY TRENCH CAPACITORS

Related Applications

This application claims the benefit of U.S. Provisional Application 60/311,801 filed August 13, 2001, the entire disclosure of which is hereby incorporated by reference.

Field of the Invention

This invention relates generally to semiconductor structures and particularly to semiconductor structures formed on strained semiconductor layers.

Background

Relaxed silicon-germanium (SiGe) virtual substrates, including a tensilely strained layer and a relaxed underlying layer, enable the production of novel silicon (Si)-, germanium (Ge)-, and SiGe-based devices such as field-effect transistors (FETs). A "virtual substrate" includes a layer of SiGe that has been relaxed to its equilibrium lattice constant (i.e., one that is larger than that of Si). This relaxed SiGe layer can be directly applied to a Si substrate (e.g., by wafer bonding or direct epitaxy) or atop a graded SiGe layer, in which the lattice constant of the SiGe material has been increased gradually over the thickness of the layer. The SiGe virtual substrate can also incorporate buried insulating layers, in the manner of a silicon-on-insulator (SOI) wafer. In order to fabricate high-performance devices on these platforms, thin strained layers of Si, Ge, or SiGe are grown on the relaxed SiGe virtual substrates. The resulting biaxial tensile or compressive strain alters the carrier mobilities in the layers, enabling the fabrication of high-speed and/or low-power devices. Utilizing both strain and bandgap engineering, modulation-doped FETs (MODFETs) and metal-oxide-semiconductor FETs (MOSFETs) may be tailored for enhanced performance analog or digital applications. However, because these devices are fabricated on Si/SiGe virtual substrates rather than the Si substrates commonly utilized for complementary MOS (CMOS) technologies, they present new processing challenges.

One processing challenge to device fabrication on Si/SiGe virtual substrates is the definition of dynamic random access memory (DRAM) trench storage capacitors. DRAM storage capacitors require high quality insulating layers for storing charge. A conventional DRAM trench storage capacitor formed on, for example, a p-type Si substrate may include an outer plate of, e.g., n-type doped Si substrate material (also referred to as the buried plate), a high-quality insulator grown on the outer plate, and an inner plate of, e.g., n-type doped

strained, and may have dislocation defects. The challenges associated with forming a good quality thermal dielectric on trench sidewalls having many defects are addressed by forming an outer plate, an insulating layer, and an inner plate by deposition processes. In some embodiments, the quality of the deposited outer plate is sufficient for the thermal growth of the insulating layer. Alternatively, an outer plate may be formed in a trench sidewall by diffusion of dopants from a sacrificial source. Subsequently, an insulating layer may be thermally grown or deposited on the outer plate. In some other embodiments, the outer plate is formed by doping the substrate region proximate the trench, either prior to or after trench formation. This doping may be performed, for example, by an implantation process (e.g., ion implantation). Alternatively, substrate layers may be doped during epitaxial formation.

In one aspect, therefore, the invention features a method for forming a trench capacitor in a semiconductor substrate. A trench is defined extending into the semiconductor substrate from a top surface of the substrate. A first conductive material is deposited in the trench to define an outer plate, and an insulating layer is formed on the outer plate. A second conductive material is deposited in the trench to define an inner plate.

One or more of the following features may also be included. The semiconductor substrate may include a layer containing germanium, with the trench extending into the germanium-containing layer. The step of forming the insulating layer may include deposition, such as chemical vapor deposition, or the insulating layer may be grown. The semiconductor substrate may include a tensilely strained layer disposed over a relaxed layer.

In another aspect, the invention features a method for forming a trench capacitor in a semiconductor substrate, in which the semiconductor substrate includes germanium. A trench is defined extending into the semiconductor substrate from a top surface of the substrate. A material including dopants is introduced into the trench. The dopants are diffused into a sidewall of the trench to define an outer plate. The material is removed from the trench, and an insulating layer is formed on the outer plate. A conductive material is deposited on the insulating layer to define an inner plate.

One or more of the following features may also be included. The material may be introduced into the trench by deposition. The material may include polysilicon. The step of removing the material comprises may include a wet etch. The step of forming the insulating layer may include thermal growth and/or deposition.

In another aspect of the invention, a method for forming a trench capacitor in a semiconductor substrate includes providing the semiconductor substrate, with the substrate

substrate, with the second region of the semiconductor substrate being electrically isolated from the first region, and the logic circuit including at least one transistor.

In another aspect, the invention features a semiconductor structure including a substrate having a first region substantially free of germanium and a second region having a layer including germanium. The structure also includes a trench capacitor disposed in the first region, the trench capacitor including an outer plate, an insulator disposed proximate the outer plate, and an inner plate disposed proximate the insulator.

One or more of the following features may be included. The second region may include a strained layer disposed over a relaxed layer. The relaxed layer may include germanium. The strained layer may include at least one of silicon, germanium, a group II element, a group III element, a group V element, and a group VI element.

In another aspect, the invention features a semiconductor structure including a trench capacitor, which itself includes a trench formed in a semiconductor substrate, the trench extending into a region of the substrate including germanium. A conductive trench sidewall has a conductivity imparted by dopants disposed therein and defining an outer plate. An insulating layer is disposed proximate the outer plate. A second conductive material is disposed in the trench proximate the insulating layer, with the second conductive material defining an inner plate.

One or more of the following features may also be included. The dopants may be diffused into the trench sidewall. The dopants may be implanted into the trench sidewall.

In another aspect, a semiconductor structure includes a trench capacitor, which itself includes a trench formed in a semiconductor substrate, with the trench extending into a region of the substrate including germanium and dopants. A conductive trench sidewall has a conductivity imparted by the dopants disposed in the region of the substrate and defining an outer plate. An insulating layer is disposed proximate the outer plate, and a second conductive material is disposed in the trench proximate the insulating layer, the second conductive material defining an inner plate.

One or more of the following features may also be included. The substrate may include a relaxed layer including germanium and dopants, and the trench may extend into the relaxed layer. The substrate may include a strained layer and the trench may extend into the strained layer.

A tensilely strained layer 18 is disposed over relaxed layer 14, sharing an interface 19 with relaxed layer 14. In an embodiment, tensilely strained layer 18 is formed of silicon. In other embodiments, tensilely strained layer 18 may be formed of SiGe, or at least one of a group II, a group III element, a group V, and a group VI element. Tensilely strained layer 18 may have a starting thickness T_3 of, for example, 50 - 300 Å.

In some embodiments, a compressively strained layer (not shown) may be disposed between relaxed layer 14 and tensilely strained layer 18. In an embodiment, the compressively strained layer includes $Si_{1-y}Ge_y$ with a Ge content (y) higher than the Ge content (x) of relaxed $Si_{1-x}Ge_x$ layer 14. The compressively strained layer may contain, for example 40 - 100% Ge and have a thickness of , e.g., 10 - 200 angstroms (Å).

A trench 20 is defined in layers 11, extending into semiconductor substrate 13 from a top surface 22 of semiconductor substrate 13. Trench 20 may be defined by, e.g., reactive ion etching (RIE). Trench 20 may have an aspect ratio of 40:1, with a width w_1 of, e.g., 0.3 μm and a depth d_1 of, e.g., 12 μm. In the illustrated embodiment, trench 20 extends through layers 11 into substrate 10.

Referring to Figure 1(b), a first conductive material is deposited in trench 20 to define an outer plate 24. First conductive material may be, for example, n-type doped polysilicon, having a thickness T_4 of, e.g., 100 - 500 Å. Outer plate 24 may be formed by deposition, such as by CVD or physical vapor deposition (PVD). Subsequently, an insulating layer 26 is formed on outer plate 24. Insulating layer 26 may be a thermally-grown material, such as silicon dioxide or nitrided silicon dioxide. Alternatively, insulating layer 26 may be deposited by, for example, plasma enhanced CVD (PECVD), LPCVD, or APCVD. In an embodiment in which insulating layer 26 is deposited, the composition of the sidewall of trench 20, e.g., outer plate 24, may not affect the quality of insulating layer 26. The deposited insulating material may be, for example, a material with a dielectric constant higher than that of silicon dioxide, such as tantalum oxide (Ta_2O_5) or silicon nitride (Si_3N_4). Insulating layer 26 may have a thickness T_5 of, e.g., 15 - 50 Å.

Referring to Figure 1(c), a second conductive material is deposited in trench 20 proximate insulator 26 to define an inner plate 28. Second conductive material may be, for example, n-doped polysilicon. A DRAM trench capacitor 30 includes outer plate 24, insulator 26, and inner plate 28.

Referring to Figure 2, in an alternative embodiment, layers 11, i.e., tensilely strained layer 18, relaxed layer 14, and graded layer 12, are sufficiently thick to completely accommodate a DRAM trench capacitor 220 including outer plate 24, insulator 26, and inner plate 28. In this

as a p-type dopant source. Dopant source 400 may be, for example, deposited by CVD. After formation of dopant source 400, a thermal anneal is performed to out-diffuse dopants from dopant source 400 into a sidewall 410 of trench 400 to define an outer plate 420. In embodiments in which layers 11 contain Ge, this thermal anneal may be performed at a temperature lower than conventionally used in silicon processing because of the greater diffusivity of n-type carriers in germanium-containing layers. The anneal may be performed, for example, at 800 - 900 °C for 30 minutes.

Referring to Figure 4(c) as well as to Figure 4(b), dopant source 400 is removed by, for example, a wet etch such as a mixture of hydrofluoric acid and water. Subsequently, insulating layer 26 is formed on outer plate 420. As discussed above with reference to Figure 1(b), insulating layer 26 may be thermally-grown silicon dioxide or nitrided silicon dioxide. Alternatively, insulating layer 26 may be deposited by, for example, PECVD, LPCVD, or APCVD. The deposited insulating material may be, for example, a material with a dielectric constant higher than that of silicon dioxide, such as Ta_2O_5 or Si_3N_4.

A conductive material is deposited on insulating layer 26 to define inner plate 28. The conductive material may be, for example, n-type doped polysilicon.

As shown in Figure 5, portions of SiGe virtual substrate layers may be doped to define the outer plate of a DRAM trench capacitor. In this embodiment, a semiconductor substrate 500 includes a plurality of layers 502 disposed over substrate 10. Layers 502 include a graded layer 505 disposed over substrate 10. Graded layer 505 may be doped and may include SiGe with a grading rate of, for example, 10% Ge/μm of thickness. During epitaxial growth, graded layer 505 may be doped with n-type dopants, such as phosphorus or arsenic. In an alternative embodiment, graded layer 500 may be doped with p-type dopants such as boron or gallium. A relaxed layer 510, disposed over doped graded layer 500, may include, for example, $Si_{1-x}Ge_x$, that may be doped with the same type of dopants as are incorporated in graded layer 500, i.e., n-type or p-type dopants. A tensilely strained layer 520 is disposed over relaxed layer 510. In an embodiment, tensilely strained layer 520 is formed of silicon. In other embodiments, tensilely strained layer 520 may be formed of SiGe, or at least one of a group II, a group III, a group V, and a group VI element. The doped layer(s), e.g., at least one of tensilely strained layer 520, relaxed layer 510, and graded layer 505, form an outer plate 540 for a subsequently formed DRAM trench capacitor (as discussed below).

A trench capacitor may be formed in a doped region, so that the doped region defines the outer plate of the trench capacitor. A trench 550 is formed by, e.g., RIE in tensilely strained

In alternative embodiments, the trench capacitors described above may be formed in layers which are either all SiGe, or are various combinations of SiGe and Si. The SiGe layers may include graded SiGe, relaxed SiGe, and/or compressively strained SiGe.

The invention may be embodied in other specific forms without departing from the spirit of essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

9. The method of claim 7, wherein the material introduced into the trench comprises polysilicon.

10. The method of claim 7, wherein the step of removing the material comprises using a wet etch.

11. The method of claim 7, wherein the step of forming the insulating layer comprises thermal growth.

12. The method of claim 7, wherein the step of forming the insulating layer comprises deposition.

13. A method for forming a trench capacitor in a semiconductor substrate, the method comprising:

providing the semiconductor substrate, said substrate comprising a layer containing germanium;

introducing dopants into a region of the substrate;

thereafter defining a trench in the substrate region, the trench extending into the germanium-containing layer and the region including the dopants defining an outer plate along a sidewall of the trench;

forming an insulating layer in the trench proximate the outer plate; and

depositing a conductive plate on the insulating layer to define an inner plate.

14. The method of claim 13, wherein the step of forming the insulating layer comprises deposition.

15. The method of claim 14, wherein the deposition is chemical vapor deposition.

16. The method of claim 13, wherein the step of forming the insulating layer comprises growth.

17. A semiconductor structure comprising a trench capacitor, which itself comprises:

a trench formed in a semiconductor substrate, the trench extending into a region of the substrate comprising germanium;

a first conductive material disposed in the trench and defining an outer plate;

an insulating layer disposed proximate the outer plate; and

26. The semiconductor structure of claim 23, wherein the trench is formed on a first region of the semiconductor substrate, further comprising:

a logic circuit disposed on a second region of the semiconductor substrate, the second region of the semiconductor substrate being electrically isolated from the first region, and the logic circuit including at least one transistor.

27. A semiconductor structure comprising:

a substrate having a first region substantially free of germanium and a second region comprising a layer including germanium; and

a trench capacitor disposed in the first region, the trench capacitor including an outer plate, an insulator disposed proximate the outer plate, and an inner plate disposed proximate the insulator.

28. The structure of claim 27, wherein the second region comprises a strained layer disposed over a relaxed layer.

29. The structure of claim 28, wherein the relaxed layer comprises germanium.

30. The structure of claim 28, wherein the strained layer comprises at least one of silicon, germanium, a group II element, a group III element, a group V element, and a group VI element.

31. A semiconductor structure comprising a trench capacitor, which itself comprises:

a trench formed in a semiconductor substrate, the trench extending into a region of the substrate comprising germanium;

a conductive trench sidewall having a conductivity imparted by dopants disposed therein and defining an outer plate;

an insulating layer disposed proximate the outer plate; and

a second conductive material disposed in the trench proximate the insulating layer, the second conductive material defining an inner plate.

32. The structure of claim 31, wherein the dopants are diffused into the trench sidewall.

33. The structure of claim 31, wherein the dopants are implanted into the trench sidewall.

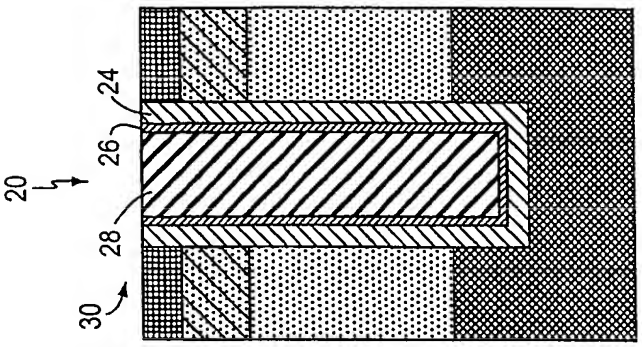


FIG. 1C

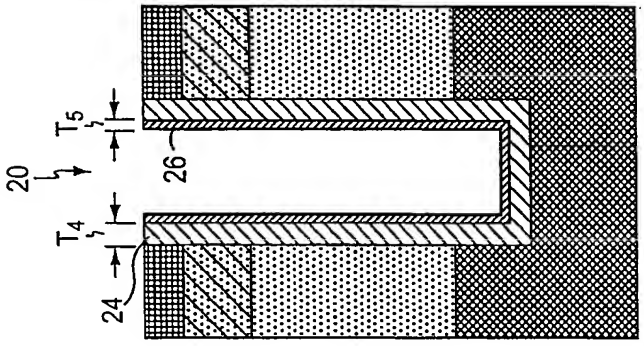


FIG. 1B

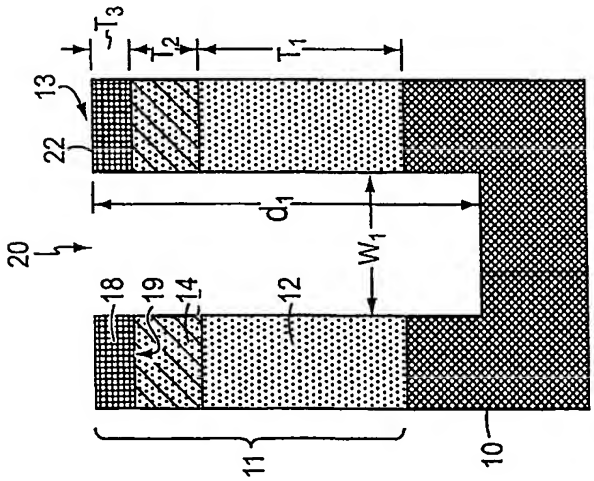


FIG. 1A

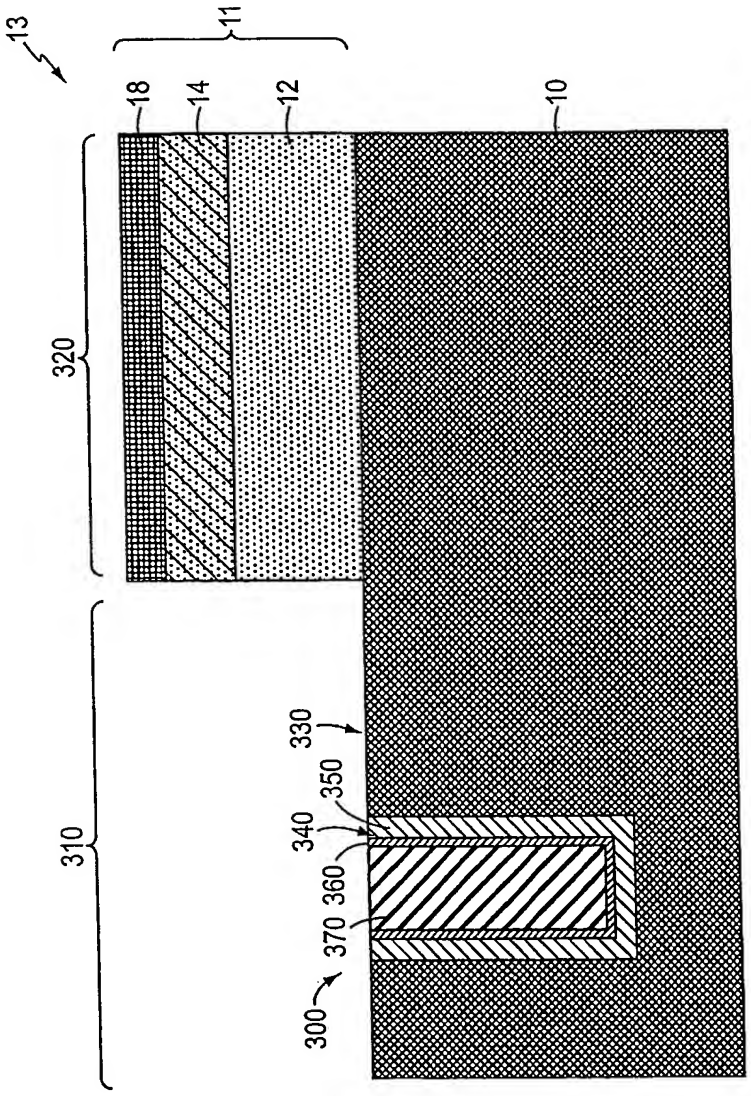


FIG. 3

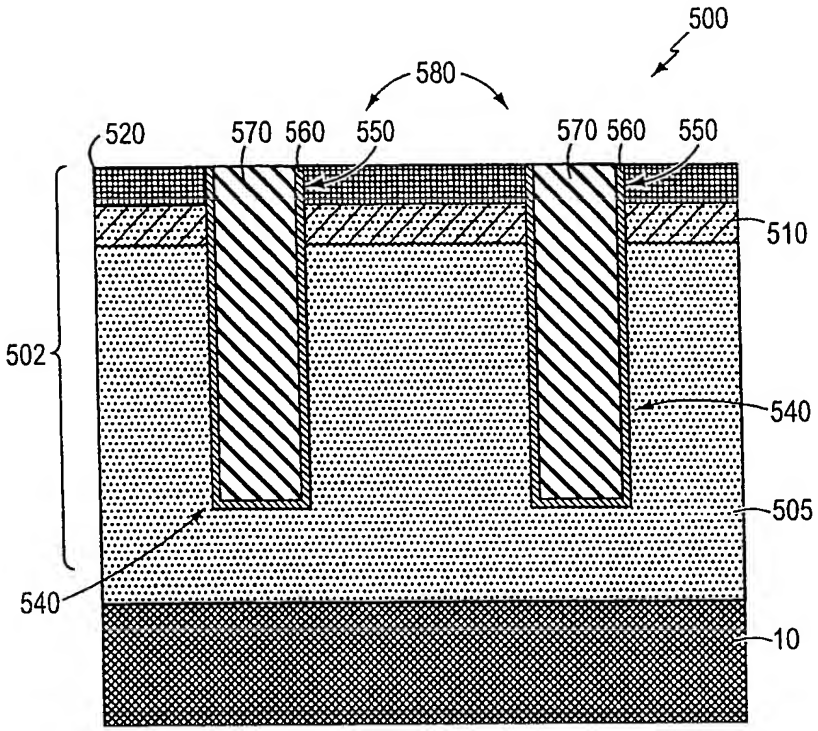


FIG. 5